What is claimed is:

1. An image sensor comprising:

a sensor unit that is made up of a plurality of pixels;

a scanning circuit having a dynamic logic circuit for outputting selection signals that select pixels from among said plurality of pixels in the sensor unit; and

a bootstrap circuit placed between the scanning circuit and the sensor unit, for holding a selection signal outputted from the scanning circuit during one horizontal scanning period, and outputting, to the sensor unit, an AND signal obtained by performing a logical AND between the held selection signal and a drive signal that specifies a timing to output the AND signal to the sensor unit.

2. The image sensor according to Claim 1,

wherein the drive signal is for electronic shutter use.

3. The image sensor according to Claim 2,

wherein the bootstrap circuit includes:

a switch connected to a selection signal line from the scanning circuit;

a boosting transistor for holding said selection signal in a gate capacitor; and

a capacitative element for boosting a gate voltage in the boosting transistor,

wherein the boosting transistor holds said selection signal in the gate capacitor by an input of said selection signal to a gate of the boosting transistor via the switch, and outputs said AND signal from one of either drain or source to the sensor unit by an input of said drive signal to the other of the drain or source.

4. The image sensor according to Claim 3,

wherein said selection signal outputted from the scanning

circuit is at high level during said one horizontal scanning period even while the gate capacitor holds said selection signal.

5. The image sensor according to Claim 4,

wherein the scanning circuit outputs said selection signal at high level during said one horizontal scanning period by use of a drive pulse that is at high level during said one horizontal scanning period.

6. The image sensor according to Claim 5,

wherein the switch is a switching transistor, and

a threshold of the gate voltage to turn on the switching transistor is smaller than a threshold of the gate voltage to turn on the boosting transistor.

7. The image sensor according to Claim 6,

wherein the switch transmits said selection signal to the gate of the boosting transistor when said switch is turned on at a time when one horizontal scanning period shifts to another horizontal scanning period.

8. The image sensor according to Claim 7,

wherein the switch is a switching transistor that is always on, and

the scanning circuit outputs said selection signal as a pulse having an arbitrary width during said one horizontal scanning period, by use of a drive pulse having said arbitrary width.

9. The image sensor according to Claim 8,

wherein the capacitative element is a gate capacitor of an enhancement-typed transistor in which drain and source are short-circuited.

10. The image sensor according to Claim 4,
wherein the switch is a switching transistor, and
a threshold of the gate voltage to turn on the switching transistor is smaller than a threshold of the gate voltage to turn on the boosting transistor.

11. The image sensor according to Claim 4,
wherein the switch transmits said selection signal to the gate of the boosting transistor when said switch is turned on at a time when one horizontal scanning period shifts to another horizontal scanning period.

12. The image sensor according to Claim4,
wherein the scanning circuit outputs the selection signal as a pulse having an arbitrary width within said one horizontal scanning period, by use of a drive pulse having said arbitrary width.

13. The image sensor according to Claim 4,
wherein the switch is a switching transistor that is always on, and
the scanning circuit outputs the selection signal as a pulse having an arbitrary width within said one horizontal scanning period, by use of a drive pulse having said arbitrary width.

14. The image sensor according to Claim 4,
wherein the capacitative element is a gate capacitor of an enhancement-typed transistor in which drain and source are short-circuited.

15. The image sensor according to Claim 3,
wherein the switch is a switching transistor, and
a threshold of the gate voltage to turn on the switching

transistor is smaller than a threshold of the gate voltage to turn on the boosting transistor.

16. The image sensor according to Claim 3,

wherein the switch transmits said selection signal to a gate of the boosting transistor when said switch is switched on at a time when one horizontal scanning period shifts to another horizontal scanning period.

17. The image sensor according to Claim 3,

wherein the switch is a switching transistor that is always on, and

the scanning circuit outputs the selection signal as a pulse having an arbitrary width within one horizontal scanning period, by use of a drive pulse having said arbitrary width.

18. The image sensor according to Claim 3,

wherein the capacitative element is a gate capacitor of an enhancement-typed transistor in which drain and source are short-circuited.

19. A driving method for an image sensor,

wherein the image sensor comprises:

a sensor unit being made up of a plurality of pixels;

a scanning circuit having a dynamic logic circuit for outputting selection signals that select pixels from among said plurality of pixels in the sensor unit; and

a bootstrap circuit which is placed between the scanning circuit and the sensor unit,

wherein the method comprises:

a holding step of holding, in the bootstrap circuit, the selection signal outputted from the scanning circuit during one

horizontal scanning period; and

an output step of outputting, to the sensor unit, an AND signal obtained by performing a logical AND between the selection signal held in the bootstrap circuit and a drive signal that specifies a timing to output the AND signal to the sensor unit.

20. A camera equipped with an image sensor,

wherein the image sensor comprises:

a sensor unit being made up of a plurality of pixels; and

a scanning circuit having a dynamic logic circuit for outputting selection signals that select pixels from among said plurality of pixels in the sensor unit,

wherein the camera comprises a bootstrap circuit placed between the scanning circuit and the sensor unit, for holding the selection signal outputted from the scanning circuit during one horizontal scanning period, and outputting an AND signal obtained by performing a logical AND between the held selection signal and a drive signal that specifies a timing to output the AND signal to the sensor unit.